UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,195	09/15/2003	Yuan-Ting Wu	MTKP0074USA	2194

27765 7590 11/03/2005

NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER	
DANG, KHANH	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 11/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,195	WU ET AL.	
	Examiner	Art Unit	
	Khanh Dang	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Jeansonne et al. (Jeansonne, US2004/0205280).

As broadly drafted, these claims do not define any structure/step that differs from Jeansonne.

With regard to claim 1, Jeansonne discloses a bridge (the multi-component device 40, connected to the host 38, is readable as a bridge for bridging the host and the peripheral devices) for a Host-Bridge-Device system, the bridge (the multi-component device 40) comprising: at lease one bridge chip (66, 70, for example) for controlling operations of the bridge; and one corresponding activation circuit (74/76, for example) for each bridge chip (66, 70, see [0024], for example), each activation circuit disabling the corresponding bridge chip after a power-on, a hardware reset, or physical disconnection from the host (it is clear from at least Fig. 4 that the activation circuit of Jeansonne disables the corresponding bridge chip when there is no connection to the

host 38 or a rest from the control signal 80, for example) and enabling the corresponding bridge chip upon reception of a predetermined protocol initialization signal (the control signal 80 or the component event signal enables the bridge chip(s), see at least [0022] and [0024] to [0028]).

With regard to claim 2, it is clear that the predetermined protocol initialization signal is a signal showing a physical connection between the host and the bridge has been built (the system of Jeansonne must be adhered to the USB/IEEE1394 specfication, which supports USB or IEEE 1394 plug and play. Therefore, when a USB or IEEE1394 component is connected to the host via the bridge chip, such component must be initialized so that it can be recognized by the host. In other words, the activation switch activates the corresponding bridge chip in response to the initialization signal from the host to the connected components), a signal from the host to reset the bridge/device (the system of Jeansonne must be adhered to the USB/IEEE1394 specification, which supports USB or IEEE 1394 plug and play. Therefore, when a USB or IEEE1394 component is connected or removed, the system is reset and a reset is signal is sent from the host to rest the bridge/components), a signal from the host to initialize the bridge/device the system of Jeansonne must be adhered to the USB/IEEE1394 specification, which supports USB or IEEE 1394 plug and play. Therefore, when a USB or IEEE1394 component is connected or removed, the system is initialized to reflect a change in network components, and the host send initialization signal to the bridge/components), or a signal from the host to acknowledge the

existence of the bridge/device (every component connected to a USB or 1394 network must be acknowledged by a signal from the USB/1394 host).

With regard to claim 3, it is clear from at least Fig. 6 and description thereof that each bridge chip comprises the corresponding activation circuit.

With regard to claim 4, it is clear that when the bridge chip of Jeansonne is disabled, the bridge chip does not control the device via the device interface pins. See also [0030]-[0031].

With regard to claim 5, it is clear that when the bridge chip is enabled, the enabled bridge chip must drive all pins of a device bus interface of the peripheral device connecting the device bus interface to the enabled bridge chip so that the enabled bridge chip controls the device bus interface. See also [0030]-[0031].

With regard to claim 6, it is clear that when the bridge chip of Jeansonne is enabled, the enabled bridge chip retains control of the device bus interface until a power-off, a hardware reset occurs, or the bridge chip has been physically disconnected from the host. See discussion above and also [0030]-[0031].

With regard to claim 7, it is clear from discussion above that the apparatus disclosed by Jeansonne comprises the bridge discussed above.

With regard to claims 8-22, see discussion regarding claims 1-7 above.

Response to Arguments

Applicants' arguments filed 9/15/2005 have been fully considered but they are not persuasive.

At the outset, Applicants are reminded that claims subject to examination will be given their broadest reasonable interpretation consistent with the specification. *In re Morris, 127 F.3d 1048, 1054-55 (Fed. Cir. 1997)*. In fact, the "examiner has the duty of police claim language by giving it the broadest reasonable interpretation." *Springs Window Fashions LP v. Novo Industries, L.P.,* 65 USPQ2d 1862, 1830, (Fed. Cir. 2003). Applicants are also reminded that claimed subject matter not the specification, is the measure of the invention. Disclosure contained in the specification cannot be read into the claims for the purpose of avoiding the prior art. *In re Sporck*, 55 CCPA 743, 386 F.2d, 155 USPQ 687 (1986).

With this in mind, the discussion will focus on how the terms and relationships thereof in the claims are met by the references. Response to any limitations that are not in the claims or any arguments that are irrelevant and/or do not relate to any specific claim language will not be warranted.

The Jeansonne 102 Rejection:

With regard to claim 1, Applicants argue that "Jeansonne et al. do not teach 'enabling the corresponding bridge chip upon reception of a predetermined protocol initialization signal.'"

Contrary to Applicants' argument, it is clear that bridge chips 66 and 70 are protocol conversion chips to provide communication translations, between different communication interfaces, such as USB, IEEE-1394, IDE, ATA, ATAPI, Floppy Disk, and so forth. Further, it is also clear that the respective bridge chip is enabled upon

receiving a "signal" representing a component event or control signal 80. Fig. 8 shows a process employed by bridge 40 comprising an endpoint selector 65. The selector may comprise a control signal (e.g., a high/low control signal), a multiplexor, an isolator switch, a hardware switch, an enable/disable control, and so forth. For example, the automatic selector may comprise an event-activated or control-signal activated isolator or switch, which is operable to enable one and disable others of the communication bridges in response to a component event or control signal. See at least [0028]. In another embodiment, the control signal 80 selectively enables end points 54 and 56 comprising protocol conversion bridge chips 66 and 70 (see at least Fig. 4 and description thereof). Since each bridge chip represents a different protocol(s), the control signal 80 or the component event signal is readable as "protocol initialization signal" to enable one of protocol conversion bridge chips 66 and 70, and disable the other.

With regard to claim 1, Applicants also argue that Jeansonne et al. does not disclose an activation circuit for "disabling the corresponding bridge chip after a power-on, a hardware reset, or a physical disconnection from the host."

At the outset, it is noted that only one of the conditions set forth in the above limitation is required. It is also noted that as drafted, the limitation "disabling" does not require a "protocol initialization signal." In any event, contrary to Applicants' argument, as set forth above regarding the enable control signal, it is clear that the end point selector 74/76 (see at least Fig. 4) also disables one of the protocol conversion bridge chip 66/70 of endpoint 54/56 at least after a physical disconnection from the host 38 or

a reset from the control signal 80. It is noted that since each bridge chip represents a different protocol(s), the control signal 80 or the component event signal is readable as "protocol initialization signal" to enable one of protocol conversion bridge chips 66 and 70, and disable the other.

With regard to claim 4, Jeansonne does not disclose "when the bridge chip is disabled, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface."

Contrary to Applicants' argument, it is clear that when the bridge chip of Jeansonne is disabled due to the fact that the end point selector 74/76 (see at least Fig. 4) disables one of the protocol conversion bridge chip 66/70 of endpoint 54/56 at least after a physical disconnection from the host 38 or a reset from the control signal 80, the bridge chip does not control the device via the device interface pins or in other words, all pins of a device bus interface connecting the device bus interface to the disabled bridge chip are set to floating so that the disabled bridge chip does not control the device bus interface.

With regard to claim 6, Applicants argue that Jeansonne does not disclose "the enabled bridge chip retains control of the device bus interface until a power-off, a hardware reset occurs, or the bridge chip has been physically disconnected from the host."

At the outset, it is noted that only one of the conditions set forth in the above limitation is required. Contrary to Applicants' argument, it is clear that in case of a

power-off condition or a physical disconnection from the host 38, the bridge chips 66 and 70 simply do not control of the device bus interface. As a matter of fact, no communications between interfaces/devices can occur when there is no power or a physical disconnection between them.

With regard to claim 12, Applicants argue that Jeansonne does not disclose "an original bus interface capable of communication between the device and the host computer system utilizing an original bus interface when all of the bridge chips are disabled."

Contrary to Applicants' argument, it is clear from at least Fig. 4 of Jeansonne that the bus 42 is capable of providing communication between the host 38 and the multi-component device 40 when bridge chips 66 and 70 of the endpoints 54 and 56 are disabled.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication should be directed to Khanh Dang at telephone number 571-272-3626.

Khanh Dang